Computer Architecture and Operating Systems Lecture 5: Assembly Programming - Branches and Memory

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## Program Structure and Memory Layout



## Labels

- Labels are symbolic names for addresses (in the .data or .text segment).
- Labels are used by control-flow instructions (branches and jumps).
"Labels are used by load and store instructions.



## Addressing

## Addresses can be represented in several ways

1. Immediate addressing

| immediate | rs1 | funct3 | rd | op |
| :--- | :--- | :--- | :--- | :--- |

2. Register addressing

3. Base addressing

| immediate | rs1 | funct3 | rd | op |
| :--- | :--- | :--- | :--- | :--- |


4. PC-relative addressing


## Program Counter

- Program Counter (PC) is a special register that stores the address of the currently executed instruction.
- When an instruction is executed, the PC is incremented by the size of the instruction (4 bytes) to point to the next instruction.
- Branch and jump instructions assign to the PC new addresses to change the control flow.
- Branch instructions use PC-relative addresses (increment or decrement current value by an offset).


## Branch Instructions

## Branch Instructions

- Branch =
- Branch $=$
- Branch <
- Branch $\geq$
beq rs1, rs2, label
bne rs1, rs2, label
blt rs1, rs2, label
bge rs1, rs2, label
- Branch < Unsigned bltu rs1, rs2, label
- Branch $\geq$ Unsigned bgeu rs1, rs2, label


## Branch Pseudo Instructions

## Branch Pseudo Instructions

- Branch unconditionally j label
- Branch = 0
- Branch $\geq 0$
- Branch >
- Branch > Unsigned
- Branch > 0
- Branch $\leq$
- Branch $\leq$ Unsigned
- Branch $\leq 0$
- Branch < 0
- Branch $\neq 0$
beqz rs1, label
bgez rs1, label
bgt rs1, rs2, label
bgtu rs1, rs2, label
bgtz rs1, label
ble rs1, rs2, label
bleu rs1, rs2, label
blez rs1, label
bltz rs1, label
bnez rs1, label


## Branches and Program Counter

-Branch instructions are PC-relative
-They add a 12-bit signed immediate to PC
-The immediate is an offset from PC to the target label

- The branch address range is $\pm 2^{12}$ (4096 $\left.\mathrm{B}=4 \mathrm{~KB}\right)$
- PC can be read with the auipc instruction main:
auipc a0, 0 \# a0 = PC + 0
li a7, 34 \# Print as hex
ecall \# Print a0


## Assembly Code for "If-Then-Else"

$$
\begin{aligned}
& \text { if_0: }
\end{aligned}
$$

## Assembly Code for "While"

while:
li a7, 5
ecall
while((t0 = read_int()) != 0) \{ print_int(t0) print_char('|n')
mv t0, a0
beqz a0, end_while
li a7, 1
ecall
li a7, 11
li a0, ' n '
ecall
j while end_while:

## Assembly Code for "For"

for:

```
for (t0 = 0; t0 < t1; ++t0) {
    print_int(t0)
    print_char('\n')
}
```

li a7, 5
ecall
mv t1, a0
mv t0, zero
next:
beq t0, t1, end for
mv aO,t0
li a7, 1
ecall
li a7, 11
li a0, '\n'
ecall
addi t0, t0, 1
j next
end_for:

## Assembly Code for Nested "For"

mv t0, zero

```
for (t0 = 0. t0 < s0. ++t0) { next_t0:
for (t0 = 0; t0 < sO; ++t0) {\longrightarrow beq t0, s0, end_for_t0
    for (t1 = 0; t0 < s1; ++t1) { me t1, zero
    for (t1 = 0; t0
        print_char(':')
        print_int(t1)
        print_int(' ')
    }
    print_char('\n')
}
next_t1:
beq t1, s1, end_for_t1
print_int(t0)
print_char(':')
print_int(t1)
print_char(' ')
addi \̄1, t1, 1
end_for_t1:
```


## Macros

Macro is a pattern-matching and replacement facility that provides a simple mechanism to name a frequently used sequence of instructions.

```
.macro print_int (%x)
li a7,1
mv a0, %x
ecall
.end_macro
    .macro read_int (%x)
li a7,5
ecall
mv %x, a0
    .end_macro
```


## Including Macro Libraries

It is possible to place macros in a library file and include it in other assembly programs.

## .include "macrolib.s"

main:

```
read_int(t0)
print_int(t0)
```

The read_int and print_int macros are defined in the macrolib.s file. The file must be in the same directory as the program.

## Macro Constants and Single-Line Macros

The .eqv directive can be used to define macro constants and single-line macros.

```
                            .eqv VAL 0x123
.eqv }X\mathrm{ t0
.eqv }Y\mathrm{ t1
.eqv SUM addi }Y,X,VA
main:
li X, 0x111
SUM
```


## Data Segment

Segment .data stores static data (global variables and constants), which are described with the following
.data directives:
.word OxDEADBEEF
.half 0x1234, 0x4567
.byte 0x98, 0x76, 0x65, 0x43
.space 8
.ascii "Hello"
.asciz "World!"
\# 32-bit value
\# 16-bit values
\# 8-bit values
\# 8 bytes of empty space
\# String
\# Zero-terminated string

## Data Alignment

Data items are aligned in memory by their size for convenience of access. This means address is multiple of size. Default alignment is as follows:

- .byte \# 1 byte
- .half \# 2 bytes
- .word \# 4 bytes

It is possible to specify a custom alignment by $2^{n}$ bytes for a next data item with the .align directive.

- .align 0 \# 1 byte
- .align 1 \# 2 bytes
- .align 2 \# 4 bytes
- .align 3 \# 8 bytes
- etc.


## Data Alignment Example

## .data

word1
.word 0x12345678
half1:
.half $0 \times 1234$
byte1:

word2:
.word 0x12345678 .align 3
half2:
.half $0 \times 1234$ .align 3
byte2:
.byte 0x12 .align 0
word3:


## Load and Store Instructions

## Load Instructions

lb t1, offset(t2) \# t1 <- sign-extended 8-bit value from address t2 + offset Ibu t1, offset(t2) \# t1 <- zero-extended 8-bit value from address t2 + offset lh t1, offset(t2) \# t1 <- sign-extended 16-bit value from address t2 + offset Ihu t1, offset(t2) \# t1 <- zero-extended 16-bit value from address t2 + offset Iw t1, offset(t2) \# t1 <- contents of address t2 + offset

## Store Instructions

sb t1, offset(t2) \# Store low-order 8 bits (byte) of t1 to address t2 + offset sh t1, offset(t2) \# Store low-order 16 bits (half) of t1 to address t2 + offset sw t1, offset(t2) \# Store contents of t1 to address t2 + offset

## Load Address Pseudo Instruction

la t2, label \# t1 <- address of label

## Load and Store Example



## Load and Store With Offset Example

| \# data[3] is a static array that stores three integer variables | $\qquad$ |
| :---: | :---: |
| int data[3]; \# x, y, z | read_int(to) sw $\mathrm{t} 0,0(\mathrm{t} 2)$ |
| $\mathrm{x}=$ read_int(); |  |
| $\mathrm{y}=\mathrm{read}_{-} \mathrm{int}() ;$ | sw $\mathrm{t} 0,4(\mathrm{t} 2)$ |
| $\mathrm{z}=\mathrm{x}+\mathrm{y}$; |  |

## Load and Store Pseudoinstruction Example



## Load and Store Pseudo Instructions

## Load Pseudo Instructions

Iw t1, (t2) \# t1 <- contents of memory at address t2
Iw t1, imm \# t1 <- contents of memory address in imm
Iw t1, label \# t1 <- contents of memory at label's address

## Store Pseudo Instructions

sw t1,(t2) \# Store t1 to address t2
sw t1, imm \# Store t1 to address in imm
sw t1, imm, t2 \# Store t1 in to address in imm using t2 as temp sw t1, label, t2 \# Store t1 to label's address using t2 as temp

For instructions lb, lbu, lh, lhu, sb, and sh similar pseudo instructions are provided.

## Any Questions?

```
                                    . text
            __start:
            cycIe:
                                addi t2, zero, 0x21
                                beq t1, t2, done
                                    slt t0, t1, t2
                                    bne tO, zero, if_less
                                    nOP
                            sub t1, t1, t2
                                j cycle
                                nOP
    if_less: sub t2, t2, t1
            j cycle
done:
    add t3,t工, zero
```

